II. REMARKS

Claims 1-20 are pending and are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Morioka et al., (U.S. Patent No. 6,611,728) in view of Shimono (U.S. Patent No. 6,308,293). Applicant traverses these rejections for the reasons stated below. Applicant does not acquiesce in the correctness of the rejections and reserves the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicant reserves the right to pursue the full scope of the subject matter of the claims in a subsequent patent application that claims priority to the instant application.

In Applicant's previous response, Applicant argued that the suspected fault list 14 of Shimono is derived from the circuit description of the LSI and test pattern 12 (see col. 8, lines 6-10) - not compared to the test pattern 12. Rather, the suspected fault list 14 is used to identify suspected circuit faults on which to perform a fault simulation (see col. 10, lines 7-19). As such, the comparison feature of claim 1 is also not taught by Shimono. Applicant further requested that the Office specifically define the "inputted set of suspected faulty device features", and the "previously studied features" of Shimono.

In the Response to Arguments in the Final Office Action, the Office provides no additional analysis, but alleges that Shimono teaches a fault diagnosis comprising "inputting suspected faulty device features and comparing suspected faulty device features with previously studied features," and specifically points to column 1, lines 38-65. However, column 1, lines 38-65 references the background section in which Shimono discusses two Japanese publications, 1-244384 (Heisei I) and 4-55776 (Heisei II). The discussion of these third party references by Shimono is effectively hearsay, and without citing the references themselves, should not be considered as prima facie evidence of obviousness. A brief review of the passages in column 1,

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lines 38-65 involve numerous ambiguities, e.g., (1) the paragraph ending at line 42 is incoherent, (2) it is unclear what is meant by "a result of a simulation performed by *assuming* suspected fault sites"; (3) it is unclear what is meant by an estimation; etc. As such, Applicant submits that the current rejection is improper since it does not rely on a cited reference, but instead relies on a vague discussion of un-cited references. Accordingly, Applicant submits that the Final Office Action was improperly issued since new grounds were raised.

Applicant further notes that regardless of the issue raised above, the cited passages of Shimono clearly fails to teach or suggest **first** "simulating the operation of the device using a simulation program" and **then** "determining a set of features in the device from the simulation that are potentially causing the failure," as recited, e.g., in the method of claim 9. Instead, the cited passages clearly teach the opposite, i.e., performing a simulation based on suspected fault sites in order to verify an estimation (see column 1, lines 46-50).

Accordingly, because the Office has essentially issued new grounds of rejection involving Heisei I and/or Heisei II, Applicant respectfully submits that either the 35 USC 103(a) rejections be withdrawn or a new Non-final action be issued with an IDS citing Heisei I and/or Heisei II.

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If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Reg. No. 40,019

Dated: 1/5/09

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